IN THE CLAIMS:

Please amend the claims as set forth below:

1. (Previously Presented) A processor comprising:

a code segment register configured to store a code segment selector locating a code segment descriptor;

a segment register configured to store a segment selector locating a segment descriptor; and

an execution core coupled to the segment register, wherein the execution core is configured to:

(i) execute a first instruction specifying the segment register, the execution core being selectively responsive to the segment descriptor during execution of the first instruction dependent on which of a plurality of protected operating modes is active in the processor, wherein an active protected operating mode of the plurality of protected operating modes is determined, at least in part, responsive to the code segment descriptor; and

(ii) update the segment register in response to a segment load instruction independent of which of the plurality of protected operating modes is active.

2. (Original) The processor as recited in claim 1 wherein, in a first protected operating mode of the plurality of protected operating modes, a virtual address has greater than 32 bits.

3. (Previously Presented) A processor comprising:

a segment register configured to store a segment selector locating a segment descriptor; and

an execution core coupled to the segment register, wherein the execution core is configured to:

(i) execute a first instruction specifying the segment register, the execution core being selectively responsive to the segment descriptor during execution of the first instruction dependent on which of a plurality of protected operating modes is active in the processor, wherein, in a first protected operating mode of the plurality of protected operating modes, a virtual address has greater than 32 bits, and wherein the execution core is not responsive to the segment descriptor if the first protected operating mode is active; and

(ii) update the segment register in response to a segment load instruction independent of which of the plurality of protected operating modes is active.

4. (Original) The processor as recited in claim 3 wherein the execution core is responsive to the segment descriptor if a different one of the plurality of protected operating modes is active.

5. (Original) The processor as recited in claim 1 further comprising a second segment register configured to store a second segment selector locating a second segment descriptor, wherein the execution core is coupled to the second segment register and is configured to execute a second instruction specifying the second segment register, and wherein the execution core is responsive to the second segment descriptor during execution of the second instruction independent of which of the plurality of protected operating modes is active.

6. (Original) The processor as recited in claim 1 wherein, prior to updating the segment register in response to the segment load instruction, the execution core is configured to check the segment descriptor for one or more exception conditions, and wherein the execution core is configured to signal an exception instead of updating the segment register if at least one of the one or more exception conditions is detected.

7. (Previously Presented) An apparatus comprising:

a first storage location corresponding to a code segment register, the first storage location storing a code segment selector locating a code segment descriptor;

a second storage location corresponding to a segment register, the second storage location storing a segment selector locating a segment descriptor; and

a processor configured to:

(i) process a first instruction specifying the segment register, the processing selectively responsive to the segment descriptor dependent on which of a plurality of protected operating modes is active, wherein an active protected operating mode of the plurality of protected operating modes is determined, at least in part, responsive to the code segment descriptor; and

(ii) update the second storage location in response to a segment load instruction independent of which of the plurality of protected operating modes is active.

8. (Original) The apparatus as recited in claim 7 wherein, in a first protected operating mode of the plurality of protected operating modes, a virtual address has greater than 32

bits.

9. (Previously Presented) An apparatus comprising:

a storage location corresponding to a segment register, the storage location storing a segment selector locating a segment descriptor; and

a processor configured to:

(i) process a first instruction specifying the segment register, the processing selectively responsive to the segment descriptor dependent on which of a plurality of protected operating modes is active, wherein, in a first protected operating mode of the plurality of protected operating modes, a virtual address has greater than 32 bits, and wherein the processing of the first instruction is not responsive to the segment descriptor if the first protected operating mode is active; and

(ii) update the storage location in response to a segment load instruction independent of which of the plurality of protected operating modes is active.

10. (Previously Presented) The apparatus as recited in claim 9 wherein the processing of the first instruction is responsive to the segment descriptor if a different one of the plurality of protected operating modes is active.

11. (Previously Presented) The apparatus as recited in claim 7 further comprising a third storage location corresponding to a second segment register, the third storage location storing a second segment selector locating a second segment descriptor, wherein the processor is configured to process a second instruction specifying the second segment register, and wherein the processing is responsive to the second segment descriptor

independent of which of the plurality of protected operating modes is active.

12. (Previously Presented) The apparatus as recited in claim 7 wherein, prior to updating the second storage location in response to the segment load instruction, the processor is configured to check the segment descriptor for one or more exception conditions, and wherein the processor is configured to signal an exception instead of updating the second storage location if at least one of the one or more exception conditions is detected.

13. (Previously Presented) A method comprising:

determining an active protected operating mode from a plurality of protected operating modes responsive, at least in part, to a code segment descriptor;

executing a first instruction specifying a segment register, the executing selectively responsive to a segment descriptor indicated by a segment selector in the segment register, the executing selectively responsive dependent on which of a plurality of protected operating modes is the active protected operating mode; and

updating the segment register in response to a segment load instruction independent of which of the plurality of protected operating modes is the active protected operating mode.

14. (Original) The method as recited in claim 13 wherein, in a first protected operating mode of the plurality of protected operating modes, a virtual address has greater than 32 bits.

15. (Previously Presented) A method comprising:

executing a first instruction specifying a segment register, the executing selectively responsive to a segment descriptor indicated by a segment

selector in the segment register, the executing selectively responsive dependent on which of a plurality of protected operating modes is active, wherein, in a first protected operating mode of the plurality of protected operating modes, a virtual address has greater than 32 bits, and wherein the executing is not responsive to the segment descriptor if the first protected operating mode is active; and

updating the segment register in response to a segment load instruction independent of which of the plurality of protected operating modes is active.

16. (Previously Presented) The method as recited in claim 15 wherein the executing is responsive to the segment descriptor if a different one of the plurality of protected operating modes is active.

17. (Original) The method as recited in claim 13 further comprising executing a second instruction specifying a second segment register configured to store a second segment selector locating a second segment descriptor, wherein the executing is responsive to the second segment descriptor independent of which of the plurality of protected operating modes is active.

18. (Original) The method as recited in claim 13 further comprising:

prior to the updating, checking the segment descriptor for one or more exception conditions; and

signalling an exception instead of the updating if at least one of the one or more exception conditions is detected.

19. (Currently Amended) A method comprising:

loading one or more segment descriptors into segment registers, the loading performed in a first protected operating mode in which at least one of the one or more segment descriptors is not used by a processor even if an instruction specifying the corresponding segment register is executed by the processor; and

branching to a code segment which establishes a second protected operating mode in which the one or more segment descriptors are used by the processor.

20. (Original) The method as recited in claim 19 wherein the loading comprises:

checking the segment descriptors for one or more exception conditions; and

exiting to an exception handler instead of loading one of the segment descriptors responsive to the checking detecting at least one of the one or more exception conditions in the one of the segment descriptors.

21. (Previously Presented) The method as recited in claim 19 wherein, in the first protected operating mode, a virtual address has greater than 32 bits.

22. (Previously Presented) The method as recited in claim 19 wherein at least another one of the segment descriptors is used if the corresponding segment register is specified by an instruction being executed in the first protected operating mode.

23. (Previously Presented) The method as recited in claim 19 further comprising creating the one or more segment descriptors in one or more segment descriptor tables.

24. (Currently Amended) A processor comprising:

a plurality of segment registers; and

an execution core coupled to the plurality of segment registers, wherein the execution core is configured to load one or more segment descriptors into one or more of the plurality of segment registers responsive to one or more segment load instructions, the loading performed in a first protected operating mode in which at least one of the one or more segment descriptors is not used by the execution core even if a first instruction specifying the corresponding segment register is executed by the execution core, and wherein the execution core is configured, responsive to a second instruction, to branch to a code segment which establishes a second protected operating mode in which the one or more segment descriptors are used by the execution core.

25. (Previously Presented) The processor as recited in claim 24 wherein the loading comprises:

checking the segment descriptors for one or more exception conditions; and

exiting to an exception handler instead of loading one of the segment descriptors responsive to the checking detecting at least one of the one or more exception conditions in the one of the segment descriptors.

26. (Previously Presented) The processor as recited in claim 24 wherein, in the first protected operating mode, a virtual address has greater than 32 bits.

27. (Previously Presented) The processor as recited in claim 24 wherein at least another one of the segment descriptors is used if the corresponding segment register is specified by an instruction being executed in the first protected operating mode.

28. (Currently Amended) An apparatus comprising:

a plurality of storage locations corresponding to a plurality of segment registers;

and

a processor coupled to the plurality of storage locations, wherein the processor is configured to load one or more segment descriptors into one or more of the plurality of segment registers responsive to one or more segment load instructions, the loading performed in a first protected operating mode in which at least one of the one or more segment descriptors is not used by the processor even if a first instruction specifying the corresponding segment register is executed by the processor, and wherein the processor is configured, responsive to a second instruction, to branch to a code segment which establishes a second protected operating mode in which the one or more segment descriptors are used by the processor.

29. (Previously Presented) The apparatus as recited in claim 28 wherein the loading comprises:

checking the segment descriptors for one or more exception conditions; and

exiting to an exception handler instead of loading one of the segment descriptors responsive to the checking detecting at least one of the one or more exception conditions in the one of the segment descriptors.

30. (Previously Presented) The apparatus as recited in claim 28 wherein, in the first protected operating mode, a virtual address has greater than 32 bits.

31. (Previously Presented) The apparatus as recited in claim 28 wherein at least another one of the segment descriptors is used if the corresponding segment register is specified by an instruction being executed in the first protected operating mode.